AMENDMENTS TO THE CLAIMS

1. (Currently amended) A semiconductor test apparatus comprising:

an input data generating unit that generates ~~the measured~~ first measurement data applied to ~~the~~ a test semiconductor device based on ~~the~~ input measurement conditions;

an expected data generating unit that generates expected data ~~based on said~~ for said input data under input first measurement data conditions;

a determination unit that compares ~~the~~ measurement result data ~~that said~~ obtained from the test semiconductor device ~~outputs to the~~ with expected data based on said measurement data~~,~~ and determines whether the function of said device is a pass or failure, and outputs the determination result data as ~~the~~ a determination result data; and

a data log system unit that writes into ~~the~~ a log memory in a time sequence ~~the~~ first associated data that includes said determination result data, first measurement result data, measurement expectation data, and measurement input data;

wherein said data log system unit writes ~~this~~ a second associated data that includes second measurement result data for a semiconductor test device that is determined as a failure into the log memory for a predetermined period even after any of said first associated data or the address of the log memory satisfy ~~the~~ preset write termination conditions that terminate the writing.

2. (Currently amended) A semiconductor test apparatus according to claim 1 wherein said data log system continues to write said second associated data including a second measurement data into the log memory over an extended time range indicated by input write extension conditions even after the write termination conditions have been satisfied,

wherein the second measurement data includes results of measurement for analysis of the failure.

3. (Currently amended) A semiconductor test apparatus according to claim 1 wherein said data log system writes said first associated data into a predetermined address of the log memory at each time unit in which ~~a determination about the pass or failure of~~ the test device is ~~made~~ a pass or a failure.

4. (Currently amended) A semiconductor test apparatus according to claim 1 wherein said log memory has a predetermined address range, and is structured so as to overwrite the ~~subsequent~~ second associated data from the head address after writing the associated data in the final address.

5. (Currently amended) A semiconductor test apparatus according to claim 1 wherein said data log system increments the address of said log memory at each time unit ~~that a determination of the pass or failure of~~ in which it is determined whether the test semiconductor device is ~~made~~ a pass or a failure, and writes in sequence said associated data.

6. (New) A semiconductor test apparatus according to claim 1, wherein said data log system decrements the address of said log memory at each time unit when it is determined that the semiconductor memory is a failure in order to carry out the second measurement and overwrites the second measurement result in said decremented address.

AMENDMENTS TO THE DRAWINGS

The attached sheet(s) of drawings includes adding the designation PRIOR ART to Figs. 7 and 8 .

Attachment: Replacement sheets